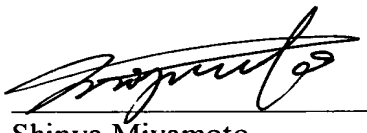
CORRECTED VERIFIED TRANSLATION

I, Shinya Miyamoto of Ark Mori Building, 13F, 12-32, Akasaka 1-chome, Minato-ku, Tokyo 107-6013, Japan, do hereby certify that I am conversant with the English and Japanese languages and am a competent translator thereof, and I further certify that to the best of may knowledge and belief the attached translation for JP Hei2002-318354 with its amendment is at true and correct translation made by me of the document in the Japanese language attached hereto.

Signed this 4th day of July, 2005



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PATENT OFFICE

Japanese Government

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Applicant:	ROHM CO., LTD.

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[DEPOSIT ACCOUNT NUMBER] 032229

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[LIST OF FILED DOCUMENTS]

[FILED DOCUMENT NAME] Specification 1

[FILED DOCUMENT NAME] Drawing 1

[FILED DOCUMENT NAME] Abstract 1

[REQUEST FOR PROOF] YES

[NAME OF DOCUMENT] Specification

[TITLE OF THE INVENTION] Semiconductor Integrated Circuit Device

[SCOPE OF CLAIM FOR PATENT]

[CLAIM 1] A semiconductor integrated circuit device having bumps provided in a terminal section on a surface of a semiconductor substrate, the bumps having electrical connection capabilities, the circuit device comprising:

electrically-non-connected dummy bumps which are disposed in the vicinity of one or more corner sections of four corners of a semiconductor chip, wherein the area of said dummy bumps projected onto a chip is larger than the area of said bumps.

[Claim 2] The semiconductor integrated circuit device according to claim 1, further comprising:

wiring which is disposed below said dummy bumps with at least one dielectric film therebetween and which is not electrically connected to said dummy bumps.

[Detailed Description of the Invention]

[DETAILED DESCRIPTION OF THE INVENTION]

[0001]

[TECHNICAL FIELD OF THE INVENTION]

The present invention relates to a semiconductor integrated circuit device having high packaging reliability.

Particularly, the invention relates to a semiconductor

integrated circuit device in which bumps having an electrical connection capability are provided at a terminal section on the surface of a semiconductor substrate and which has electrically-non-connected dummy bumps.

[0002]

[PRIOR ART]

Performance enhancement of electronic devices has recently been pursued, and a semiconductor integrated circuit packaged in the devices is required to have high performance and complicated features. Means for enabling high-density packaging is sought particularly for a semiconductor integrated circuit device to be provided in small equipment, such as a portable data terminal or portable cellular phone.

[0003]

For these reasons, a semiconductor integrated circuit device has hitherto adopted a chip geometry which essentially does not involve plastic sealing. There has hitherto been adopted a method for providing projections, such as bumps, on terminals of a chip and mounting the chip to a substrate by means of flip chip bonding. Specifically, when a semiconductor integrated circuit device is packaged, there is adopted a method for placing a chip opposite an object of connection, such as a substrate, and pressing the chip directly on the substrate by way of anisotropic conductive particles (ACP) or a conductive material.

[0004]

In this case, in response to a request for slimming down a chip, the back of the chip is ground. As a result, the chip comes to be warped or susceptible to variations in thickness. Horizontal positions of the bumps formed on the surface of the chip are displaced (see Fig. 7A).

One of the four corners of the chip often comes into contact with the substrate before a counterpart does, because of variations in the height of bumps or the precision of a bonding machine used for bonding a chip on the substrate (see Fig. 7B).

Consequently, when the chip is mounted, bumps located around the four corners of the chip are subjected to heavier load stress than that imposed on bumps located along lines or in the center section of the chip. With a view toward protecting the bumps or an electrical circuit on the chip by hindering occurrence of an unbalance in load stress, electrically-non-connected dummy bumps have hitherto been provided (as described in JP-A-8-46313 and JP-UM-T-4-94732).

[0005]

In recent years, because of an improvement in performance of an LSI; particularly, colorization embodied by an LCD driver an increase in the number of terminals associated with an increase in the size of a screen, and a finer semiconductor process, miniaturization of a chip area cannot be achieved

unless intervals between bumps are made narrower than they are now. In association with this tendency, the area of an individual bump also comes to be smaller, and hence there is no alternative but to increase the number of dummy bumps to be disposed at each of the corners of one chip.

[0006]

[PROBLEMS TO BE SOLVED BY THE INVENTION]

The related-art semiconductor integrated circuit device is subjected to a limit in narrowing the interval between the bumps, because of a particle size (3 μm to 5 μm) of the anisotropic conductive particles (ACP). A distance of at least 10 μm to 15 μm must be ensured between the bumps.

In contrast, individual bumps are required to be substantially identical in size with each other for electrically connecting the chip with the substrate without fail through use of the ACP. As shown in Fig. 8, the respective bumps must assume a narrow shape. For these reasons, a so-called invalid area (hatched in Fig. 8) of a space existing between the bumps becomes larger. Accordingly, an increase in the number of dummy bumps merely results in the area where the dummy bumps are disposed being increased in relation to the total area of the bumps, thereby imposing a limitation on downsizing of a chip.

[0007]

[MEANS AND OPERATION FOR SOLVING THE PROBLEMS]

Claim 1 of the invention is characterized by providing a semiconductor integrated circuit device having bumps provided in a terminal section on a surface of a semiconductor substrate, the bumps having electrical connection capabilities, the circuit device comprising: electrically-non-connected dummy bumps which are disposed in the vicinity of one or more corner sections of four corners of a semiconductor chip, wherein the area of the dummy bumps projected onto a chip is larger than the area of the bumps.

[0008]

According to the semiconductor integrated circuit device of claim 1, the dummy bumps located in the vicinity of the corner sections of the semiconductor chip are larger than the bumps that are located around them and have electrical capabilities. An area which is located between the dummy bumps and has hitherto been taken as an open space can also be used as an area for dummy bumps. Thus, the area on the semiconductor chip can be used effectively. As a result, the area on the semiconductor chip to be used for placing dummy bumps becomes smaller than that required in the related art. Hence, the area of the semiconductor chip can be made small.

[0009]

The semiconductor integrated circuit device according to claim 2 of the invention is characterized by the semiconductor integrated circuit device of claim 1, further comprising wiring which is disposed below the dummy bumps with at least one dielectric film therebetween and is not electrically connected to the dummy bumps.

[0010]

According to the semiconductor integrated circuit device of claim 2, wiring which is not electrically connected to the dummy bumps can be placed below dummy bumps located around the corner sections of the semiconductor chip. Hence, the area on the semiconductor chip that has hitherto been used solely for dummy bumps can also be effectively used for wiring. Consequently, the area of the semiconductor chip can be made much smaller.

[0011]

[EMBODIMENT]

An embodiment of a semiconductor integrated circuit device of the invention will be described hereinbelow by reference to Figs. 1 through 6.

[0012]

Fig. 1 is a view showing the entirety of a chip of a semiconductor integrated circuit device to be used for describing the invention. The semiconductor integrated

circuit device chip 1 has bumps 6 arranged so as to surround an unillustrated internal circuit. In the embodiment, bumps are arranged along four sides of a chip 1 of the semiconductor integrated circuit device surrounding the internal circuit. In an alternative configuration, no bumps 6 are provided along one or two specific lines, and a circuit or wiring is provided instead.

[0013]

Figs. 2, 3, 4, and 5 are enlarged views showing a chip corner section 5 enclosed by broken lines in Fig. 1 as a representative of four corners of the semiconductor integrated circuit device chip 1. The drawings will be described hereinbelow.

[0014]

Fig. 2 is a view showing the layout of related-art bumps. There are provided circuit connection bumps 3 connected to an unillustrated internal circuit, and two dummy bumps 2 which are placed for each line, between the corner section of the chip 1 of the semiconductor integrated circuit device and the bumps 3. There can be obtained a load capacity effect of an area corresponding to the area occupied by a total of four circuit connection bumps 3. An inside of the area enclosed by broken lines corresponds to the area on the chip 1 of the semiconductor integrated circuit device ensured for dummy bumps.

[0015]

Fig. 3 is a bump layout view showing the first embodiment. There are provided the circuit connection bumps 3 connected to the unillustrated internal circuit, and one dummy bump 2a which is placed for each line, between the corner section of the chip 1 of the semiconductor integrated circuit device and the bumps 3. The area of the dummy bump 2a is approximately double that of the circuit connection bump 3. There can be obtained a load capacity effect of an area corresponding to the area occupied by a total of four circuit connection bumps 3. The inside of the area enclosed by broken lines corresponds to the area on the chip 1 of the semiconductor integrated circuit device ensured for dummy bumps. A load capacity effect identical with that achieved by the layout of the related-art bumps shown in Fig. 2 is achieved by use of a smaller area.

[0016]

Fig. 4 is a bump layout view showing a second embodiment. There are provided the circuit connection bumps 3 connected to the unillustrated internal circuit, and one dummy bump 2b which is placed at the corner section of the chip 1 of the semiconductor integrated circuit device and assumes a shape, the shape avoiding a circuit wiring 4 and not being rectangular. The area of the dummy bump 2b is four times or more that of the circuit connection bump 3. For this reason, there can be obtained a load capacity effect larger than that obtained from

the area occupied by the four circuit connection bumps 3. The inside of the area enclosed by broken lines corresponds to the area on the chip 1 of the semiconductor integrated circuit device ensured for dummy bumps. A load capacity effect identical with that achieved by the first embodiment shown in Fig. 3 is achieved by use of a smaller area.

[0017]

Fig. 5 is a view showing a third embodiment. There are provided the circuit connection bumps 3 connected to the unillustrated internal circuit, and one rectangular dummy bump 2c which is placed at the corner section of the chip 1 of the semiconductor integrated circuit device so as to overlap with a portion of the circuit wiring 4. The area of the dummy bump 2c is larger than that of the dummy bump of the second embodiment shown in Fig. 4. Hence, there can be obtained a load capacity effect which is much greater than that achieved in the second embodiment shown in Fig. 4.

[0018]

The load capacity effect achieved when the dummy bumps of the invention are formed on the chip will now be described by reference to Figs. 6(a) and 6(b). Fig. 6(a) is a front view showing a positional relationship between typical bumps and dummy bumps on a chip. Fig. 6(b) is a graph showing an increase in the area of dummy bumps when the number of dummy bumps is increased stepwise in the manner of one, two, three, ... and when

the width of the dummy bump is expanded freely. As can be seen from the graph, the load capacity effect of the dummy bump can be remarkably improved by a stepwise or gradual increase in the area of the dummy bump.

[0019]

[EFFECT OF THE INVENTION]

According to a semiconductor integrated circuit device of the invention, dummy bumps which are larger in area than circuit connection bumps connected to an internal circuit can be ensured in areas on a chip of a semiconductor integrated circuit device, the areas being ensured for dummy bumps smaller than related-art dummy bumps. Hence, a load capacity effect which is equal to or greater than that imposed on the area of a related-art chip can be achieved by means of a chip area smaller than that of the related-art chip.

Adoption of a geometry, in which dummy bumps are provided on circuit wiring, enables a chip area much smaller than a related-art chip area to achieve a load capacity effect which is equal to or greater than that achieved by the related-art chip area.

[BRIEF DESCRIPTION OF THE DRAWINGS]

[FIG. 1]

A chip view of a semiconductor integrated circuit device having bumps provided thereon.

[FIG. 2]

A chip view of a semiconductor integrated circuit device having related-art bumps provided thereon

[FIG. 3]

A chip view of a semiconductor integrated circuit device having bumps of a first embodiment of the invention provided thereon.

[FIG. 4]

A chip view of a semiconductor integrated circuit device having bumps of a second embodiment of the invention provided thereon.

[FIG. 5]

A chip view of a semiconductor integrated circuit device having bumps of a third embodiment of the invention provided thereon.

[FIG. 6]

A descriptive view for describing a load capacity effect derived from an increase in the area of dummy bumps.

[FIG. 7]

A view for describing problems arising at the time of bonding of a chip.

[FIG. 8]

A descriptive view showing a change in the shape of a bump.

[DESCRIPTION OF THE REFERENCE NUMERALS]

1 SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE CHIP

2, 2a, 2b, 2c DUMMY BUMPS

3 CIRCUIT CONNECTION BUMP

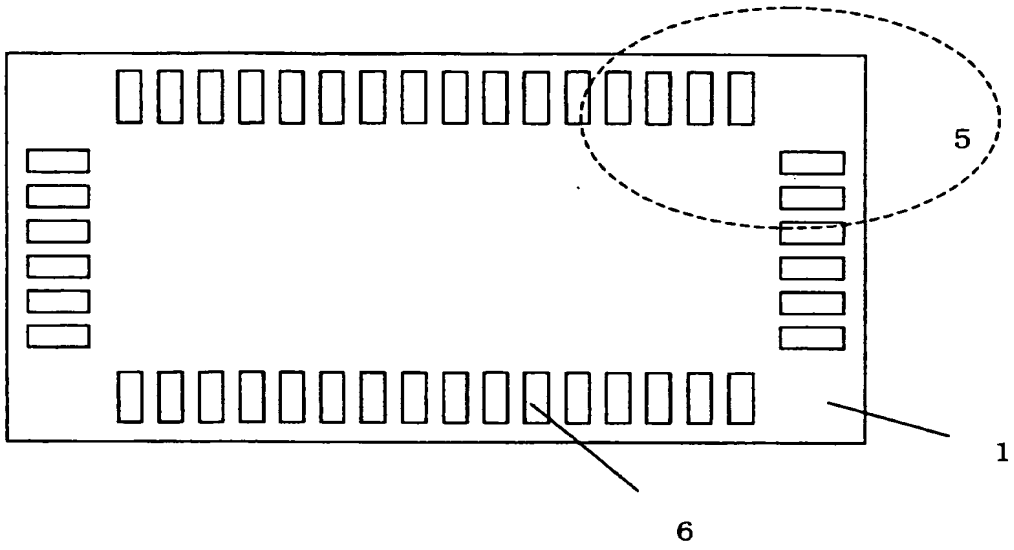
4 CIRCUIT WIRING

5 ENLARGED VIEW OF CORNER SECTION OF CHIP

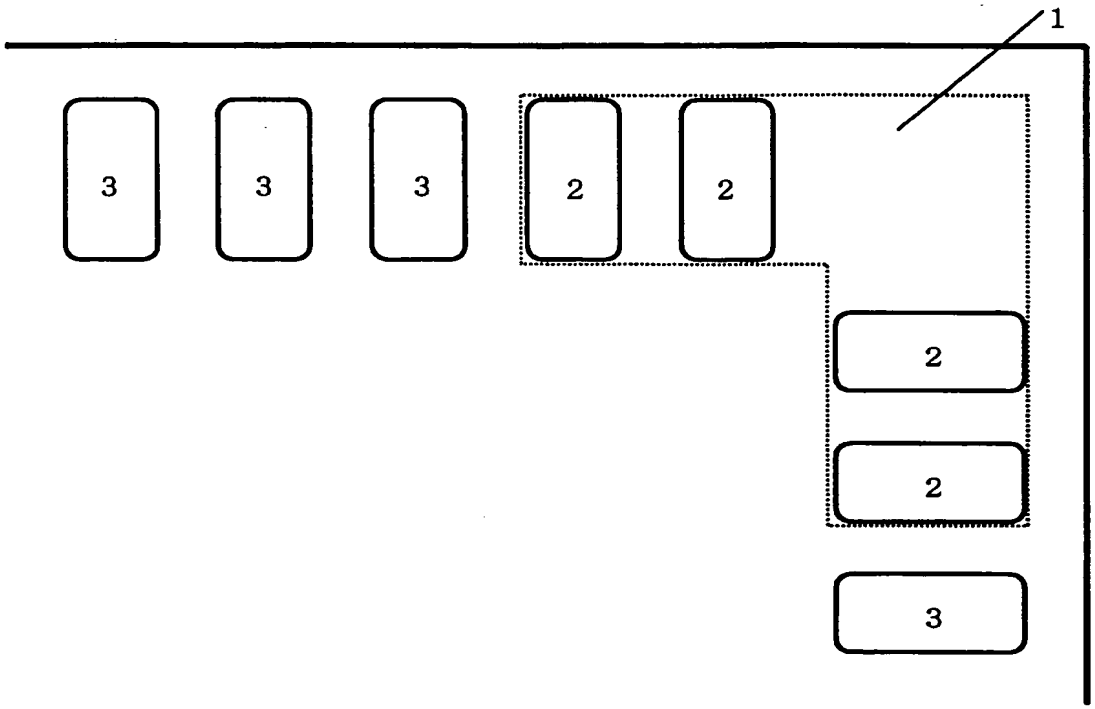
6 BUMP

[NAME OF DOCUMENT] Drawing

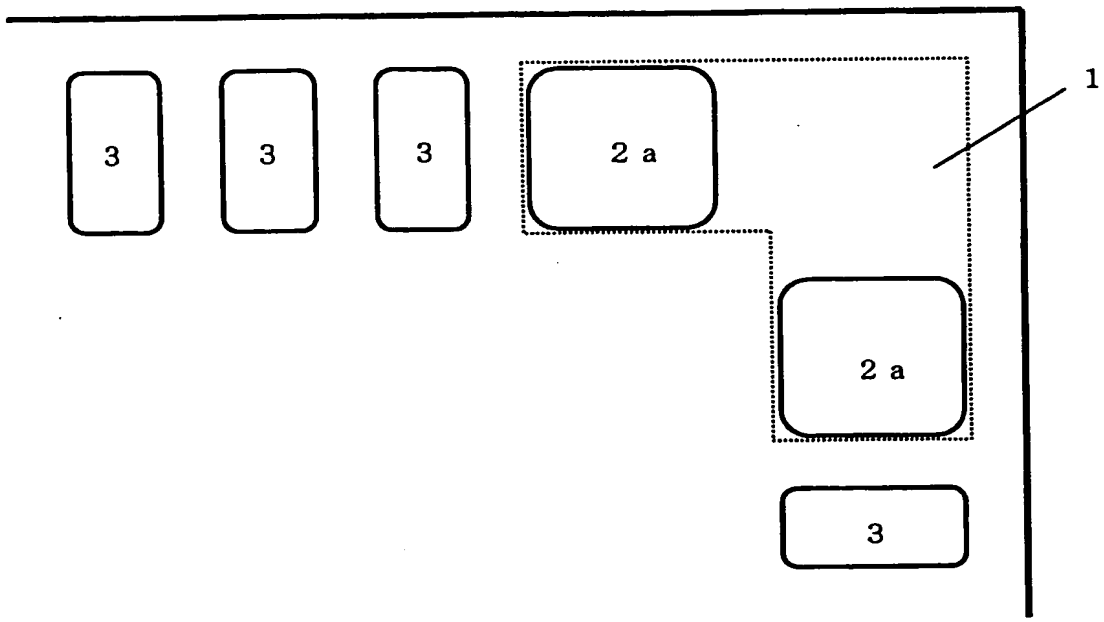
[FIG. 1]



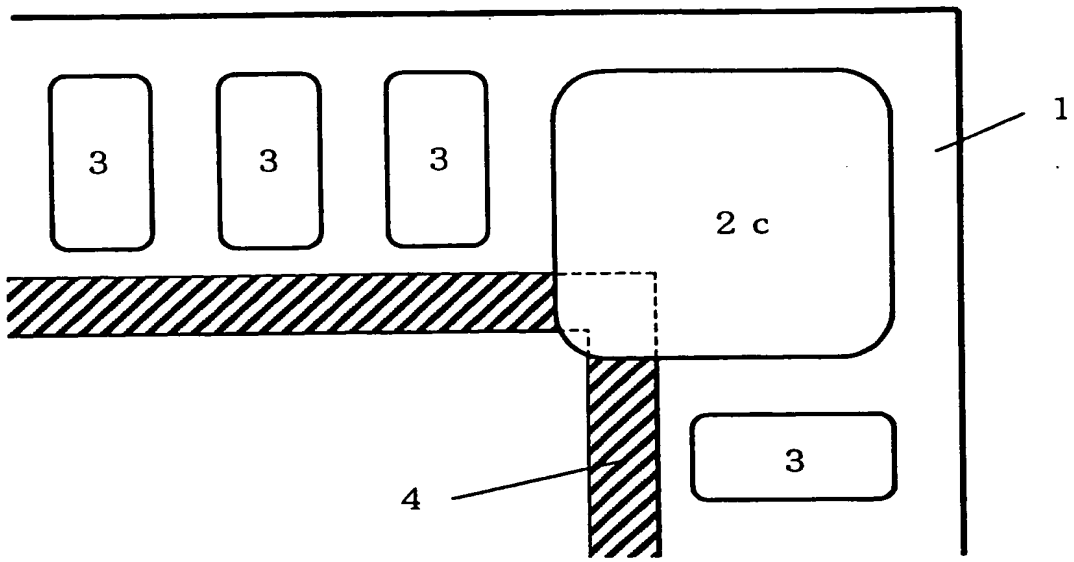
[FIG. 2]



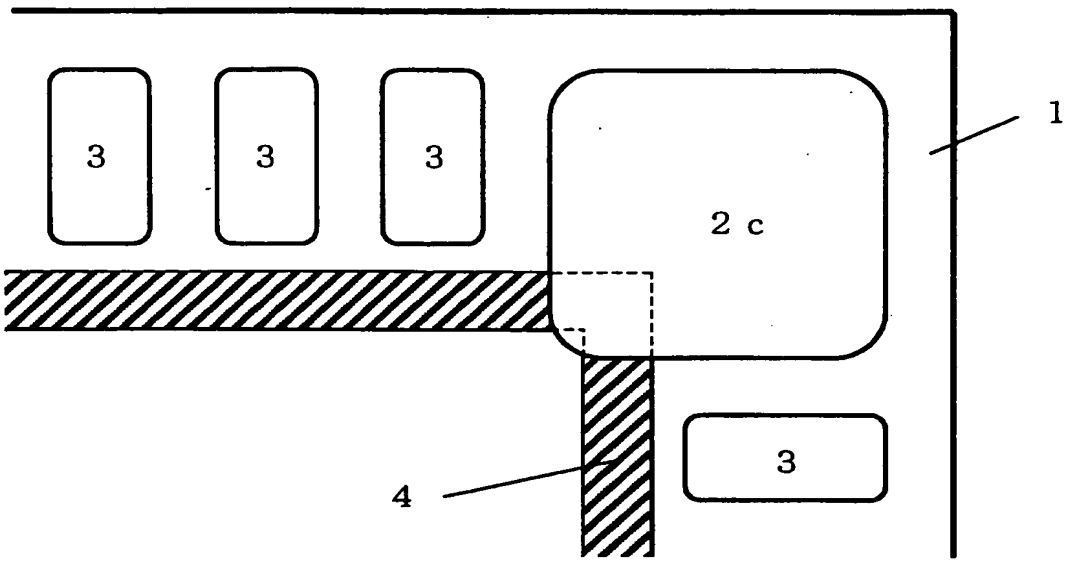
[FIG. 3]



[FIG. 4]

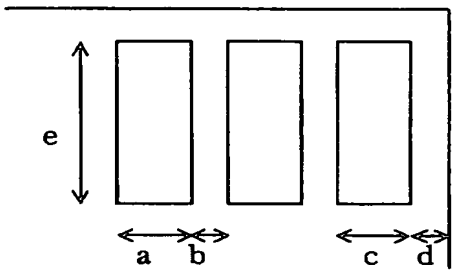


[FIG. 5]



[FIG. 6]

(a)

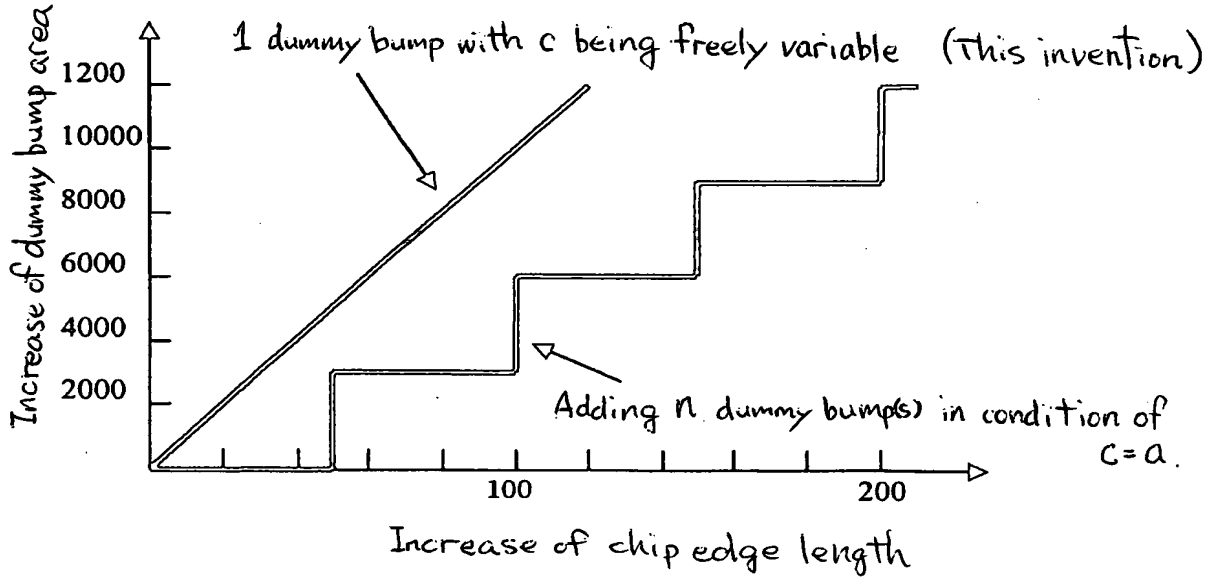


a : Width of typical bump
b : Width between the bumps
c : Width of dummy bump
d : Width between chip edge and bump

Length of chip edge

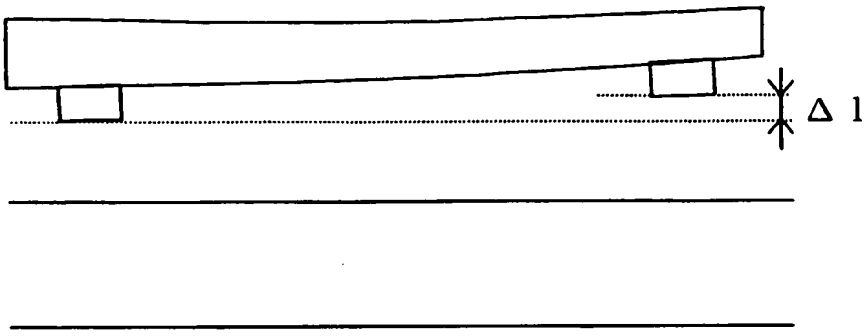
for instance
a = 3 0
b = 2 0
d = 2 0
e = 1 0 0

(b)

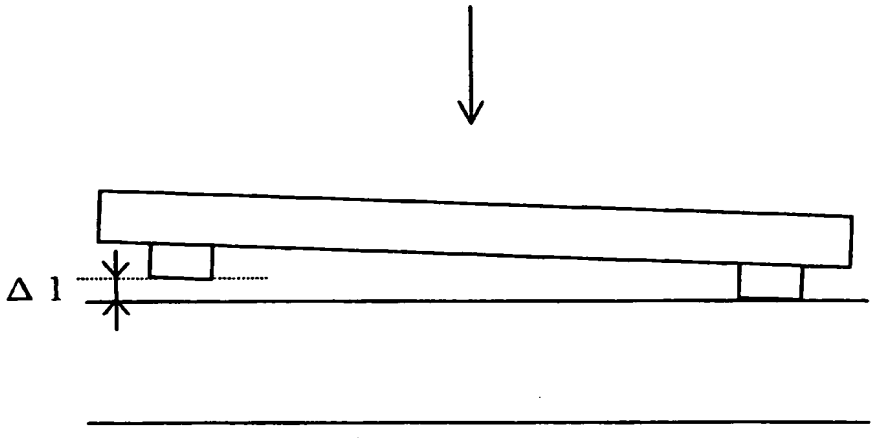


[FIG. 7]

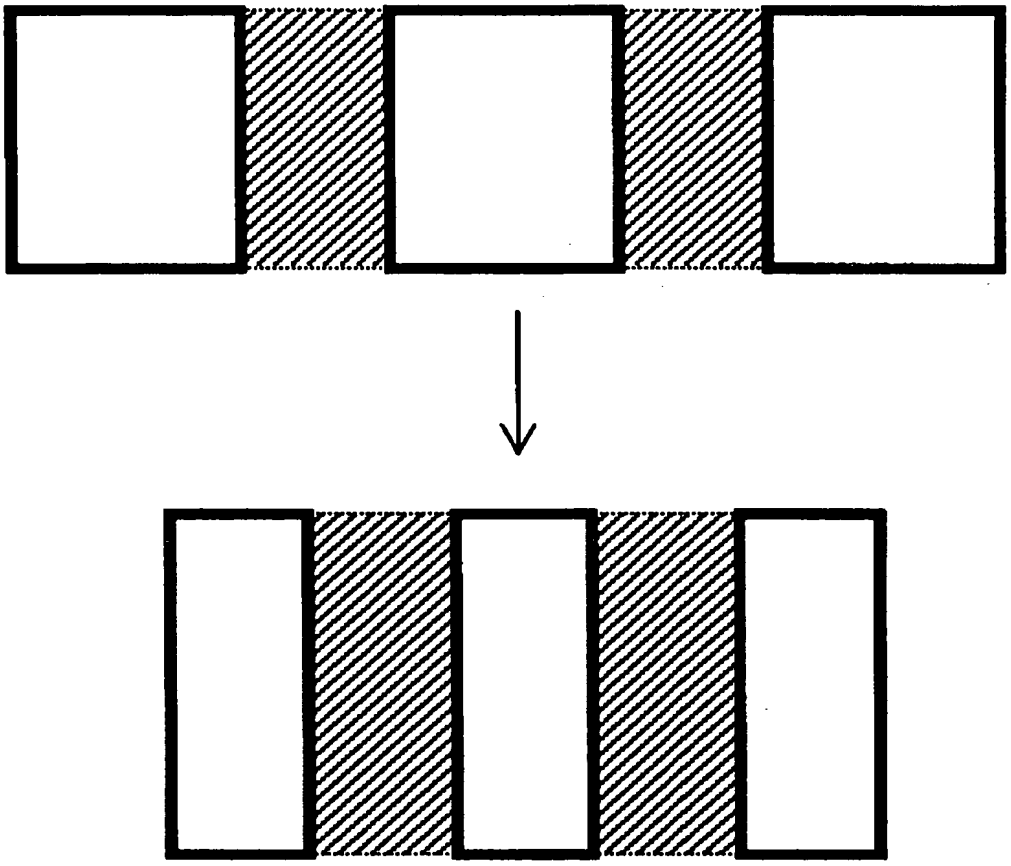
(a)



(b)



[FIG. 8]



[NAME OF DOCUMENT] Abstract

[ABSTRACT]

[OBJECT]

A semiconductor integrated circuit device which requires high packaging density adopts a method for forming bumps in a terminal section of a semiconductor chip and bonding the semiconductor chip directly on a substrate. In this case, in order to prevent damage to the semiconductor integrated chip, which would otherwise be caused by bonding pressure employed at the time of bonding operation, non-connected dummy bumps are provided at corner sections of the semiconductor chip. Even when the dummy bumps are provided, there arises a necessity for preventing an increase in the size of the semiconductor chips, which would otherwise arise when the dummy bumps are provided on the chip.

[SOLVING MEANS]

The area of dummy bumps projected on a chip is made larger than the area of ordinary bumps which have electrical capabilities and are projected onto the chip.

[SELECTED DRAWING] FIG. 3

[DOCUMENT NAME] Amendment

[REFERENCE NUMBER] 02-00361

[DATE OF FILING] October 31, 2002

[ADDRESS] Commissioner, Patent Office Esq.

[INDICATION OF CASE]

[APPLICATION NUMBER] Patent 2002-318354

[APPLICANT FOR PATENT]

[IDENTIFICATION NO.] 000116024

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[CONTACT NAME] Intellectual Property Department

[LIST OF AMENDMENT 1]

[AMENDED DOCUMENT NAME] Drawing

[AMENDED ITEM] FIG. 4

[MEANS FOR AMENDMENT] Modification

[AMENDED CONTENT] 1

[REQUEST FOR PROOF] YES

[FIG. 4]